AKRG COLLEGE OF ENGINEERING & TECHNOLOGY

(Approved By A.I.C.T.E., New Delhi and Affiliated to JNTUK, KAKINADA)

NALLAJERLA, W.G.Dt., (A.P)-534112

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

III B.Tech – I Semester **Regulation – R13**

DIGITAL SYSTEM DESIGN & DICA LABORATORY

The students are required to design and draw the internal structure of the following Digital Integrated Circuits and to develop VHDL source code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary synthesizer. Further, it is required to verify the logic with necessary hardware.

LIST OF EXPERIMENTS:

1. Realization of Logic Gates

2. 3 to 8 Decoder- 74138

3. 8*1 Multiplexer-74151 and 1*2 De-multiplexer-74155

4. 4-Bit Comparator-7485.

5. D Flip-Flop- 7474

6. Decade Counter- 7490

7. 4 Bit Counter-7493

8. Shift Register-7495

9. Universal shift register-74194/195

10. Ram (16*4)-74189 (read and write operations)

11. ALU